# Contact Electrification Field-Effect Transistor

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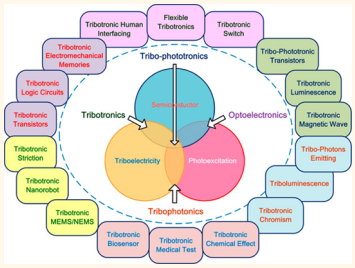
**ABSTRACT** Utilizing the coupled metal oxide semiconductor field-effect transistor and triboelectric nanogenerator, we demonstrate an external force triggered/controlled contact electrification field-effect transistor (CE-FET), in which an electrostatic potential across the gate and source is created by a vertical contact electrification between the gate material and a "foreign" object, and the carrier transport between drain and source can be tuned/controlled by the contact-induced electrostatic potential instead of the traditional gate voltage. With the two contacted frictional layers vertically separated by 80 $\mu$m, the drain current is decreased from 13.4 to 1.9 $\mu$A in depletion mode and increased from 2.4 to 12.1 $\mu$A in enhancement mode at a drain voltage of 5 V. Compared with the piezotronic devices that are controlled by the strain-induced piezoelectric polarization charged at an interface/junction, the CE-FET has greatly expanded the sensing range and choices of materials in conjunction with semiconductors. The CE-FET is likely to have important applications in sensors, human–silicon technology interfacing, MEMS, nanorobotics, and active flexible electronics. Based on the basic principle of the CE-FET, a field of tribotronics is proposed for devices fabricated using the electrostatic potential created by triboelectrification as a "gate" voltage to tune/control charge carrier transport in conventional semiconductor devices. By the three-way coupling among triboelectricity, semiconductor, and photoexcitation, plenty of potentially important research fields are expected to be explored in the near future.




**KEYWORDS:** contact electrification · field-effect transistor · triboelectric nanogenerator · electrostatic potential · tribotronics

A field-effect transistor (FET) is a device that uses an electric field to tune/control the charge carrier transport in a semiconductor material, which has a wide range of applications in integrated circuits and flexible electronics.[1,2] As the FET has a structure of three terminals, an externally supplied gate voltage is needed for controlling the drain–source current.[3–6] Due to the lack of an interaction mechanism between the external environment and electronic device, the mechanical transducer based on the FET cannot directly convert a mechanical stimulation/triggering into a control electrical signal in the FET structure.[7,8] In order to establish the mechanosensation of the semiconductor devices, piezoelectric materials can be used in FETs to generate an internal electric control signal due to the piezoelectric polarization charges created at the interface region by applying a strain.[9,10] For the piezoelectric semiconductor materials such as ZnO, GaN, and CdS with wurtzite or zinc blende structures, the coupling between piezoelectric polarization and semiconductor properties has resulted in the emerging field of piezotronics since 2007,[11–16] which has enormous applications, including but not limited to artificial intelligence, human–computer interaction, biomedicine, and communication.[17–22]

Recently, the invention of a triboelectric nanogenerator (TENG) has provided an effective approach to convert ambient mechanical energy into electricity.[23–28] The working principle of the TENG is based on the coupling of contact electrification and electrostatic induction. Contact-induced charge transfer between two materials with opposite tribopolarity results in a potential difference when they are separated. This potential difference is an inner electrical signal created by the external mechanical force, which could be used as a gate signal to tune/control the carrier transport characteristics in FET as the same effect as applying a gate voltage.

Here in this work, we developed an external force-triggered contact electrification field-effect transistor (CE-FET), which consists of a metal oxide semiconductor field-effect transistor (MOSFET) and a mobile

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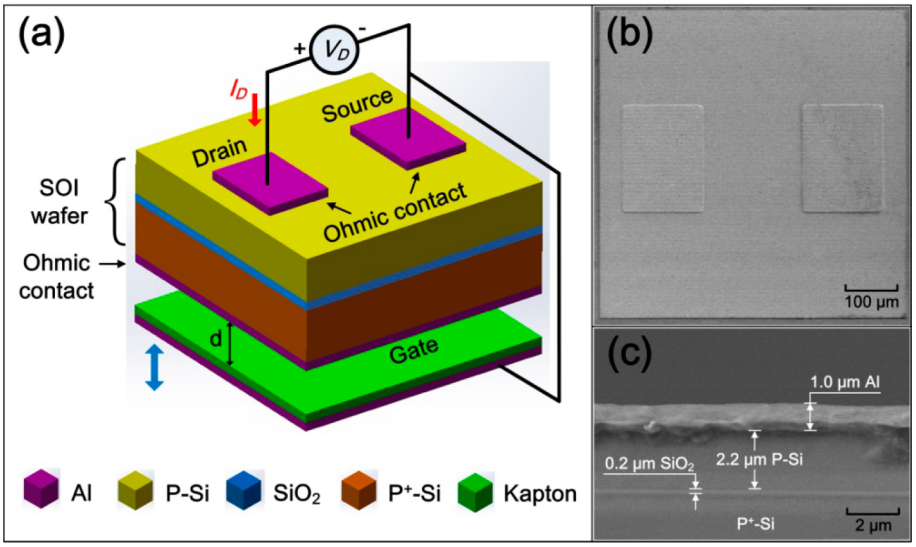


**Figure 1. Schematic illustration of the contact electrification field-effect transistor. (a) Structure of the CE-FET based on a SOI wafer with heavy-doped silicon substrate and a mobile layer for vertical contact separation. (b) Top view of the CE-FET. (c) Partial cross-sectional view of the CE-FET.**

layer for contact electrification. With the process of contact and separation between the mobile electrode and gate area of the MOSFET, the working mechanism of the CE-FET was demonstrated in two different modes. This design can generate an inner electrostatic potential in the device as a gate voltage to tune/control the carrier transport between the drain and source instead of the traditional gate voltage in the FET. Owing to the direct interaction mechanism between the external environment and electronic device, the CE-FET is likely to have important applications in sensors, human–silicon technology interfacing, MEMS, nanorobotics, and active flexible electronics. By coupling the semiconductor with triboelectricity, a field of tribotronics is proposed.

The basic structure of the CE-FET is composed of a back gate silicon-on-insulator (SOI) MOSFET and a mobile layer, as schematically illustrated in Figure 1a. In the fabrication of the CE-FET device, a SOI wafer as the sandwich structure is selected. The top silicon layer is p-type, 2.2 $\mu$m thick, and is used as the conduction channel of the CE-FET. The two 1.0 $\mu$m thick aluminum pads are deposited on the surface and annealed to form Ohmic contacts, serving as the drain and source electrodes. The buried silicon dioxide layer is 0.2 $\mu$m thick and used as the gate oxide. The silicon substrate is p-type, 500 $\mu$m thick, and heavy doped with a resistivity lower than 0.005 $\Omega\cdot$cm. An aluminum layer is then deposited on the bottom of the silicon substrate with Ohmic contact as the gate electrode. The mobile layer is assembled next to the gate electrode, which consists of a piece of Kapton film with the aluminum electrode deposited on the back side. It can vertically contact and separate with the gate electrode by the external force. The gate electrode is completely off an external voltage source, and the mobile aluminum electrode is connected to the source electrode. The drain and source electrodes are connected with a voltage source, and holes are transported from the drain electrode to the source electrode in the conduction channel. The SEM images of the CE-FET in the top view and partial cross-sectional view are shown in Figure 1b,c.

The CE-FET in this work presents a different mechanism and working principle from the conventional FET configuration, which is based on the back gate MOSFET, triboelectrification, and electrostatic induction. The depletion mode of the device is shown in Figure 2a. For the vertical contact separation of the mobile layer, the aluminum layer of the gate electrode and the Kapton film form a pair of frictional layers with a certain gap in the original state. When the mobile layer is first contacted with the aluminum layer as driven by an external force, the electrons are injected from the aluminum layer into the surface of the Kapton film since Kapton is much more triboelectrically negative than aluminum according to the triboelectric series,[29] leaving net positive electrostatic charges on the aluminum layer and net negative electrostatic charges on the Kapton film. The gate voltage is not influenced at this moment, and the width of the conduction channel is the same as the width of the top silicon layer. When the Kapton film is gradually separated from the aluminum layer as the external force is vertically released, the electric field formed by the triboelectric charges in the vertical direction induce the electron flow from the mobile electrode to the source electrode, forming an inner electric field voltage across the gate and source electrodes. When the external force is completely released and the gap between the two frictional layers returns to the original state, more electrons flow from the mobile electrode to the source electrode and the inner electric field

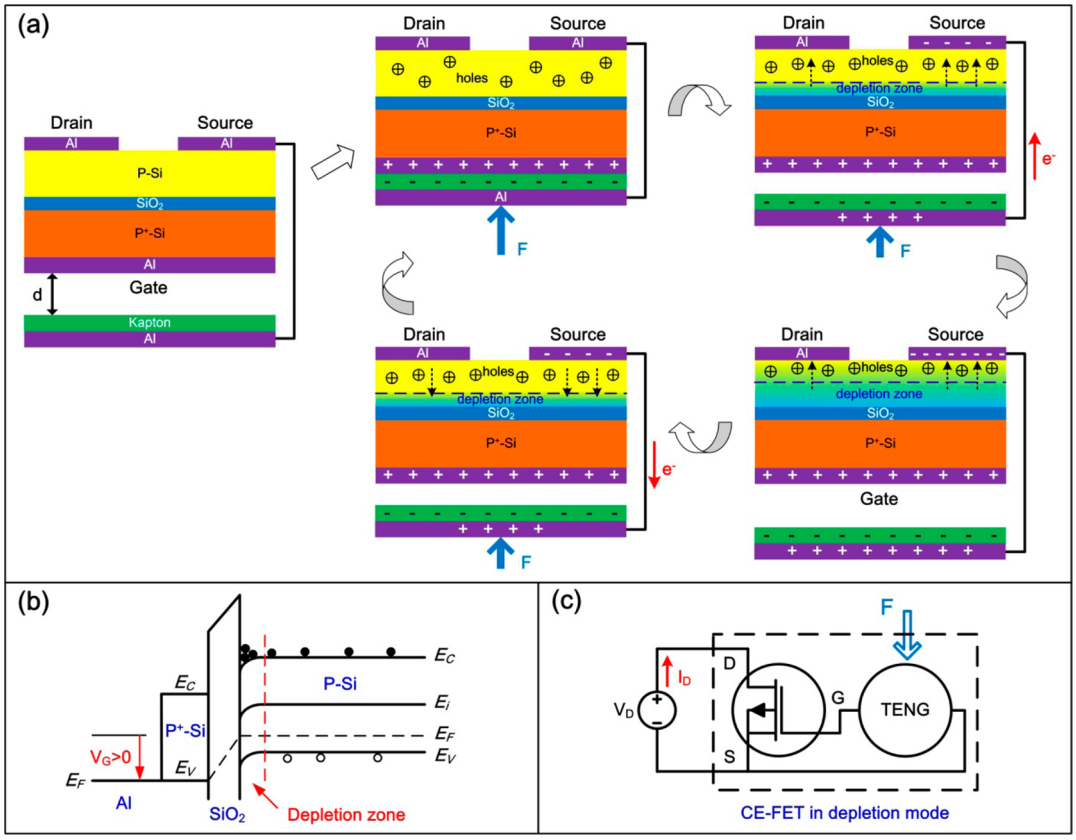


**Figure 2. Schematic working principle of the CE-FET in depletion mode. (a) Change of the gate voltage and channel width in the CE-FET with the vertical distance of the mobile layer. (b) Energy diagram illustrating the MIS capacitor in the CE-FET at the positive gate voltage. (c) Equivalent circuit of the CE-FET in depletion mode.**

reaches the maximum. In this process, the inner electric field is equivalently applied on a metal insulator semiconductor (MIS) capacitor in the MOSFET as a gate voltage due to the extremely low resistivity of the silicon substrate, which is illustrated in the energy diagram shown in Figure 2b. Therefore, an inner charge polarization is generated in the top silicon layer, which attracts electrons and repels the holes in the bottom of the silicon layer. As holes are the majority carriers in the p-type silicon, a depletion zone will be formed in this area, which will decrease the width of the conduction channel and thus the drain current. When the external force is vertically applied again and the Kapton film gradually approaches the aluminum layer, the electrons flow back from the source electrode to the mobile electrode with decreasing inner gate voltage. When the two frictional layers are contacted again, all of the electrons flow back to the mobile electrode and the inner gate voltage is decreased to zero. In this process, the inner charge polarization is depressed, which will increase the width of the conduction channel and the drain current. Therefore, the inner gate voltage can be generated and controlled by the external force, which has the same effect as applying a gate voltage. The equivalent circuit of the CE-FET in depletion mode is shown in Figure 2c. As the gap between two frictional layers and the inner positive gate voltage by the external force increases, the drain current decreases in the depletion mode. The relationship between the inner positive gate voltage $V_G$ and the gap $d$ is analyzed using Guass Theorem in the Supporting Information, which can be described by the following equation:

$$V_G = \frac{\varepsilon_K \cdot Q_0 \cdot d}{\varepsilon_0 \cdot \varepsilon_K \cdot S_0 + \varepsilon_0 \cdot C_{MIS} \cdot d_K + \varepsilon_K \cdot C_{MIS} \cdot d} \quad (1)$$

where $Q_0$ is the frictional surface charge quantity, $S_0$ is the frictional surface area, $\varepsilon_0$ and $\varepsilon_K$ are the dielectric constant of vacuum and Kapton, respectively, $d_K$ is the thickness of the Kapton film, and $C_{MIS}$ is the MIS capacitance.

The working principle of the CE-FET in the enhancement mode is illustrated in Figure 3a. Different from the structure in the depletion mode, the Kapton film is attached to the back side of the gate electrode and the mobile layer is only a piece of aluminum film, which can vertically contact with and separate from each other by an external force and form a pair of frictional layers with a certain gap in the original state. When the mobile electrode is first contacted with the Kapton film by the external force, net positive charges are left on the aluminum film and net negative charges are left on the Kapton film. The gate voltage and the channel carrier concentration are still not influenced at this

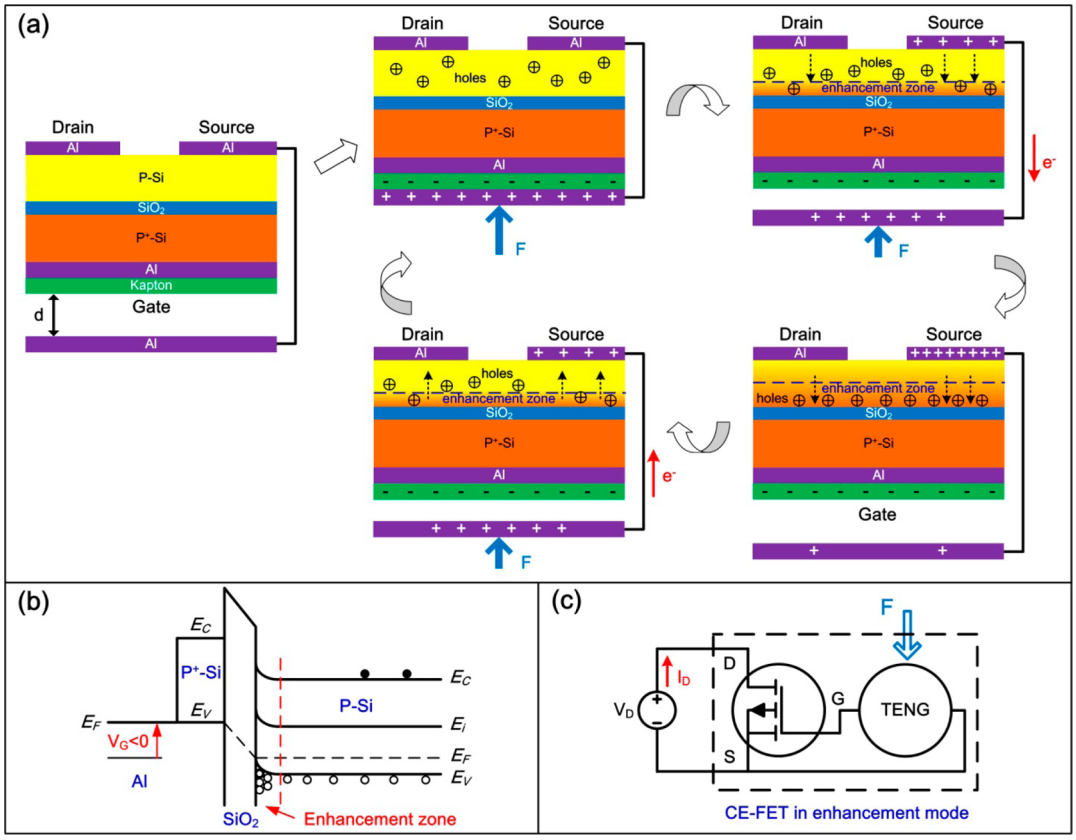


**Figure 3. Schematic working principle of the CE-FET in enhancement mode. (a) Change of the gate voltage and channel carrier concentration in the CE-FET with the vertical distance of the mobile layer. (b) Energy diagram illustrating the MIS capacitor in the CE-FET at the negative gate voltage. (c) Equivalent circuit of the CE-FET in enhancement mode.**

moment. When the mobile electrode is gradually and vertically separated from the Kapton film to the original state as the external force is released, the electrons flow from the source electrode to the mobile electrode and an inner negative gate voltage is generated. Figure 3b illustrates the energy diagram of the MIS capacitor at the negative gate voltage. In this process, an inner charge polarization generated in the top silicon layer attracts the holes but repels the electrons in the bottom of the silicon layer. Therefore, an enhancement zone will be formed in this area, which will increase the conduction channel carrier concentration and the drain current. When the external force is vertically applied again and the aluminum film is gradually approaching the Kapton film to the contact state, the electrons flow back from the mobile electrode to the source electrode with decreasing inner gate voltage. In this process, the inner charge polarization is depressed, which will decrease the conduction channel carrier concentration and drain current. Therefore, the inner gate voltage can be generated and controlled by the external force, as well, but with an opposite effect and tendency in this mode. The equivalent circuit of the CE-FET in enhancement mode is shown in Figure 3c. As the gap between two frictional layers and the inner negative gate voltage by the external force increases, the drain current is increased in the enhancement mode. The relationship between the inner negative gate voltage $V_G$ and the gap $d$ are also analyzed in the Supporting Information, which can be described by the following equation:

$$V_G = -\frac{\varepsilon_K \cdot Q_0 \cdot d}{\varepsilon_0 \cdot \varepsilon_K \cdot S_0 + \varepsilon_0 \cdot C_{MIS} \cdot d_K + \varepsilon_K \cdot C_{MIS} \cdot d} \quad (2)$$

## RESULTS AND DISCUSSION

The characteristics of the MOSFET are measured first by applying an external voltage to the gate electrode of the CE-FET, which is schematically illustrated in Figure 4a. Figure 4b shows the $I_D-V_D$ output characteristics with different $V_G$ from −5 to 0 V, and Figure 4c shows the $I_D-V_G$ transfer characteristics at a drain voltage of 5 V. The measured results fit well to the back gate MOSFET theory,[30] which indicate that the drain current is decreased with increasing gate voltage. When the gate voltage is less than about −2 V, the drain current can be significantly tuned/controlled by the gate voltage.

The device of the CE-FET is fixed in a positioning system, and the vertical distance between the two frictional layers can be controlled accurately by the external force. The characteristics of the CE-FET in the depletion mode are measured, and the $I_D-V_D$ output characteristics with different vertical distances

from 0 to 80 $\mu$m are shown in Figure 5a. Figure 5b shows the $I_D$ output characteristics at a drain voltage of 5 V with the different vertical distances, and the inset plots $I_D$–$d$ transfer characteristics. The experimental results indicate that the drain current is decreased with increasing vertical distance, which shows a good agreement with the theoretical analysis in Figure 2a. When the vertical distance is less than about 60 $\mu$m, the drain current can be significantly tuned/controlled by the external force. Compared with the MOSFET characteristics in Figure 4c, the variable distance by the external force has produced a similar transfer curve for the CE-FET, which has successfully replaced the role played by the external gate voltage. It is worth noting that the inner gate electrode suffers from a negative voltage in the state when the vertical distance is zero, which might be due to the self-owned initial negative charges on the Kapton film surface that might exist when the device was fabricated.

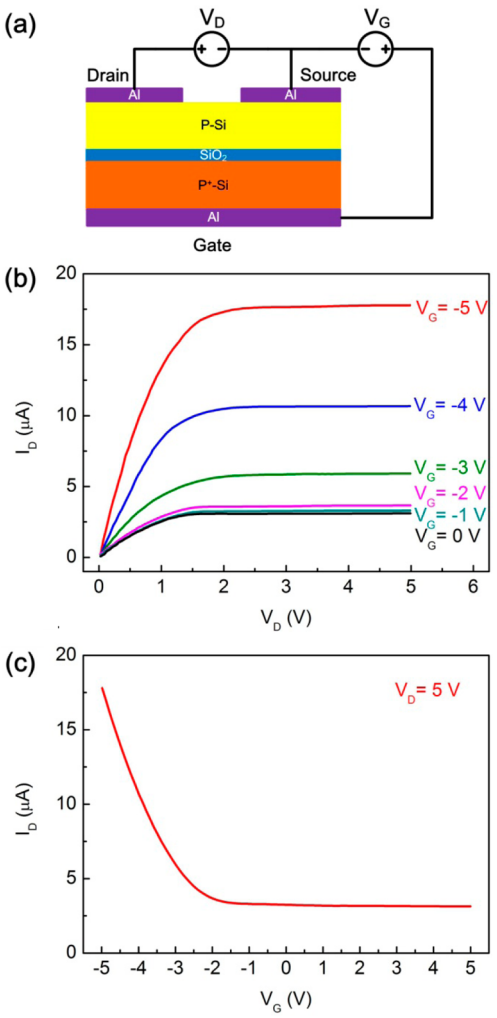


**Figure 4. Characteristics of MOSFET based on a SOI wafer with 2.2 $\mu$m channel width and 200 $\mu$m channel length. (a) Schematic circuit diagram of the MOSFET. (b) $I_D$–$V_D$ output characteristics with different $V_G$. (c) $I_D$–$V_G$ transfer characteristics at a drain voltage of 5 V.**

The characteristics of the CE-FET in the enhancement mode are measured, as well, and the $I_D$–$V_D$ output characteristics with different vertical distances from 0 to 80 $\mu$m are shown in Figure 6a. Figure 6b shows the $I_D$ output characteristics at a drain voltage of 5 V with the different vertical distances, and the inset plots $I_D$–$d$ transfer characteristics. The experimental results indicate that the drain current is increased with increasing vertical distance, which is consistent with the theoretical analysis in Figure 3a. When the vertical distance is more than about 40 $\mu$m, the drain current can be significantly tuned/controlled by the external force. Compared with the characteristics in the depletion mode, the variable distance by the external force has also produced a similar transfer curve for the CE-FET but with an opposite tendency in this mode.

The experimental results in both modes validate that an inner gate voltage can be created in the CE-FET by an external force and contact electrification, which acts as a gate voltage for tuning/controlling the transport of charge carriers through the conduction channel. The direction of the inner gate voltage depends on the different mode, and the value depends on the vertical distance between the two frictional layers. By applying an external force to the device to gate the carrier transport, a direct interaction mechanism between the external environment and electronic device has

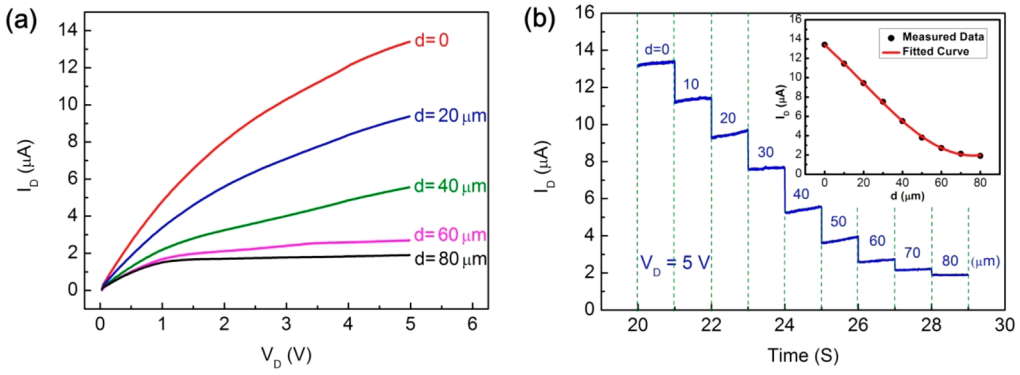


**Figure 5. Characteristics of CE-FET in depletion mode. (a) $I_D$–$V_D$ output characteristics with different vertical distances. (b) $I_D$ output characteristics at a drain voltage of 5 V with different vertical distances. The inset is the $I_D$–$d$ transfer characteristics.**

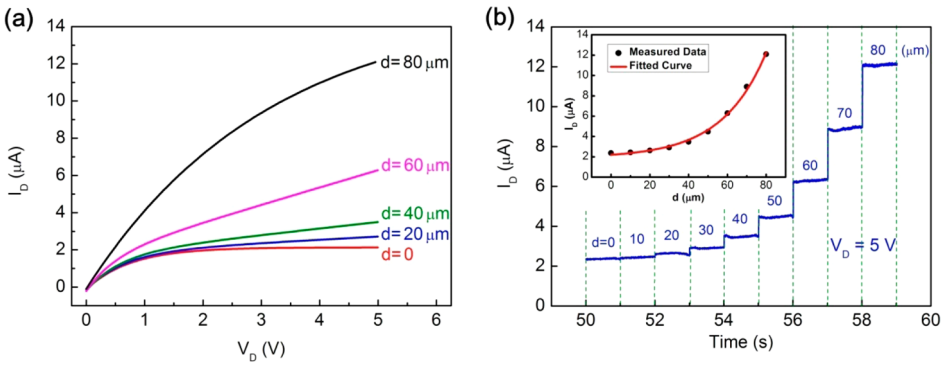


**Figure 6. Characteristics of the CE-FET in enhancement mode. (a) $I_D$–$V_D$ output characteristics with different vertical distances. (b) $I_D$ output characteristics at a drain voltage of 5 V with different vertical distances. The inset is $I_D$–$d$ transfer characteristics.**

**TABLE 1. Comparison of Traditional FET, Piezotronic Transistor, and Contact Electrification Field-Effect Transistor**

| | field-effect transistor | piezotronic transistor | CE-FET |
|---|---|---|---|
| control | external applied voltage controlling channel width | self-generated inner piezopotential controlling interface/junction | self-generated inner electrostatic potential controlling channel width |
| structure | 3-terminal (S, D, G) | 2-terminal | 2-terminal |
| gate | voltage | strain/mechanical deformation | contact/friction/force/mechanical displacement |
| sensing range | none | small | large |
| speed | fast (GHz) | slower (kHz, MHz) | slower (kHz, MHz) |
| materials | general semiconductor (Si, Ge...) | piezoelectric semiconductor (ZnO, GaN...) | general semiconductor (Si, Ge...) |
| applications | amplification, variable resistor, electronic switch | human/environmental interfacing, sensors, MEMS, flexible electronics, piezotronics, piezophotonics, piezo-phototronics, piezotromagnetism | human/environmental interfacing, sensors, MEMS, flexible electronics, tribotronics, tribophotonics, tribo-phototronics, tribotromagnetism |

been established, which provides a new approach for sensors, human–silicon technology interfacing, MEMS, nanorobotics, and active flexible electronics.

A comparison of traditional FET, piezotronic transistor, and CE-FET is presented in Table 1. Like the piezotronic transistor, the CE-FET is a two-terminal semiconductor device in which the external mechanical force can replace the traditional third terminal of FET and directly create an inner electric field to tune/control the current carrier transport characteristics. The difference is that the self-generated inner piezopotential controls the barrier height of the pie$_z$otronic transistor, while the self-generated inner electrostatic potential controls the channel width of the CE-FET as in the conventional FET. Compared with the piezotronic transistor with a limited strain sensing range,[17,18] the tuning/controlling performance of the CE-FET depends on the vertical distance, triboelectric charge density, and MOSFET characteristics, which can have a larger sensing range for the external environment. Furthermore, the selected materials for the CE-FET can be expanded to general semiconductors and any materials for contact electrification, far more than the choice of materials for piezotronic transistors. Therefore, the CE-FET could have wider application prospects in conjunction with the conventional semiconductor devices.

The CE-FET is based on the MOSFET and contact electrification effect, which can be used as fundamental components in novel triboelectronic devices and systems. We call this tribotronics, a new field of research and applications in flexible electronics. Tribotronics is about the devices fabricated using the electrostatic potential created by triboelectrification as a "gate" voltage to tune/control charge carrier transport in the semiconductor. Tribotronics is a field by coupling the semiconductor with triboelectricity, which is an extension of piezotronics first proposed in 2007,[11] and also a profound application of TENG first proposed in 2012.[23]

Figure 7 schematically shows the three-way coupling among triboelectricity, semiconductor, and photoexcitation, which is the basis of tribotronics (triboelectricity–semiconductor coupling), tribophotonics (triboelectricity–photon excitation coupling), optoelectronics, and tribo-phototronics (triboelectricity–semiconductor–photoexcitation). Besides the well-known field of optoelectronics, tribophotonics is a research field of light-emitting phenomenon on the materials of triboelectrification,[31,32] and tribo-phototronics is a research field further coupled with tribotronics and tribophotonics. These new fields can derive plenty of potentially important directions and applications in various disciplines such as material, mechatronics,

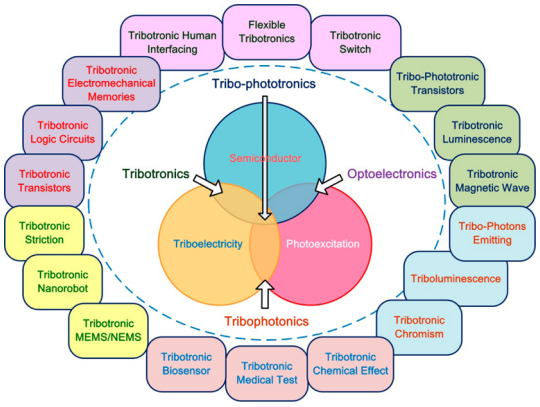


**Figure 7. Schematic diagram showing the three-way coupling among triboelectricity, semiconductor, and photoexcitation, which is the basis of tribotronics (triboelectricity–semiconductor coupling), tribophotonics (triboelectricity–photon excitation coupling), optoelectronics, and tribophototronics (triboelectricity–semiconductor–photoexcitation). Plenty of potentially important directions and applications are projected and expected to be explored in the near future.**

information, automation, environment, chemistry, biomedicine, and so on, which are projected in Figure 7 and are expected to be explored in the near future.

## CONCLUSIONS

By coupling the FET and contact electrification effect, an external force-triggered CE-FET composed of a back gate SOI MOSFET and a mobile layer is developed. With the triboelectrification and electrostatic induction, an inner gate voltage is created by the external force and used for controlling the charge carrier transport through the conduction channel, which can replace the traditonal external gate voltage. In both depletion and enhancement modes, it is validated that the charge carrier transport process in CE-FET can be tuned/gated by applying an external force to the device. The CE-FET has established a direct interaction mechanism between the external environment and electronic device, which is likely to have important applications in sensors, human–silicon technology interfacing, MEMS, nanorobotics, and active flexible electronics.

Based on the CE-FET as a fundamental component, tribotronics is proposed as a field that couples triboelectricity with semiconductors, which is about the devices fabricated using the external force to gate the charge carrier transportation in the semiconductor. Compared to piezotronics, tribotronics has greatly expanded the sensing range and choices of materials in conjunction with a general semiconductor, which is an extension of piezotronics. By the three-way coupling among triboelectricity, semiconductor, and photoexcitation, plenty of important directions and applications are expected to be explored in the near future.

## METHODS

**Fabrication of the Contact Electrification Field-Effect Transistor.** First, a SOI wafer as a sandwich structure was prepared and selected. The top silicon layer of the SOI wafer was p-type and 2.2 $\mu$m in thickness. The buried silicon dioxide layer was 0.2 $\mu$m thick, and the silicon substrate was p-type, 500 $\mu$m thick and heavy doped with a resistivity lower than 0.005 $\Omega\cdot$cm. Then, part of the top silicon layer was masked, and two 1.0 $\mu$m thick aluminum pads were deposited by RF sputtering on the surface as drain and source electrodes. Similarly, a 1.0 $\mu$m thick aluminum layer was deposited by RF sputtering on the bottom of the silicon substrate as the gate electrode. After that, the device was annealed to form Ohmic contacts between the aluminum electrodes with both the top silicon and substrate. The mobile layer was fabricated based on a piece of aluminum film, which was vertically forced by the external force and resilience force. The Kapton film was attached to the surface of the mobile aluminum film in the depletion mode, while the back side of the gate electrode was attached in the enhancement mode.

*Conflict of Interest:* The authors declare no competing financial interest.

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*Supporting Information Available:* Analysis of the relationship between the inner gate voltage and the gap is included. This material is available free of charge *via* the Internet at http://pubs.acs.org.

## REFERENCES AND NOTES

1. Crone, B.; Dodabalapur, A.; Lin, Y. Y.; Filas, R. W.; Bao, Z.; LaDuca, A.; Sarpeshkar, R.; Katz, H. E.; Li, W. Large-Scale Complementary Integrated Circuits Based on Organic Transistors. *Nature* **2000**, *403*, 521–523.
2. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-Temperature Fabrication of Transparent Flexible Thin-Film Transistors Using Amorphous Oxide Semiconductors. *Nature* **2004**, *432*, 488–492.
3. Ahn, J. H.; Kim, H. S.; Lee, K. J.; Jeon, S.; Kang, S. J.; Sun, Y.; Nuzzo, R. G.; Rogers, J. A. Heterogeneous Three-Dimensional Electronics by Use of Printed Semiconductor Nanomaterials. *Science* **2006**, *314*, 1754–1757.
4. Javey, A.; Nam, S.; Friedman, R. S.; Yan, H.; Lieber, C. M. Layer-by-Layer Assembly of Nanowires for Three-Dimensional, Multifunctional Electronics. *Nano Lett.* **2007**, *7*, 773–777.
5. Nam, S.; Jiang, X.; Xiong, Q.; Ham, D.; Lieber, C. M. Vertically Integrated, Three-Dimensional Nanowire Complementary Metal-Oxide-Semiconductor Circuits. *Proc. Natl. Acad. Sci. U.S.A.* **2009**, *106*, 21035–21038.
6. Bryllert, T.; Wernersson, L. E.; Froberg, L. E.; Samuelson, L. Vertical High-Mobility Wrap-Gated InAs Nanowire Transistor. *IEEE Electron Device Lett.* **2006**, *27*, 323–325.
7. Someya, T.; Sekitani, T.; Iba, S.; Kato, Y.; Kawaguchi, H.; Sakurai, T. A Large-Area, Flexible Pressure Sensor Matrix with Organic Field-Effect Transistors for Artificial Skin Applications. *Proc. Natl. Acad. Sci. U.S.A.* **2004**, *101*, 9966–9970.
8. Someya, T.; Kato, Y.; Sekitani, T.; Iba, S.; Noguchi, Y.; Murase, Y.; Kawaguchi, H.; Sakurai, T. Conformable, Flexible, Large-Area Networks of Pressure and Thermal Sensors with Organic Transistor Active Matrixes. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 12321–12325.

9. Dahiya, R. S.; Metta, G.; Valle, M.; Adami, A.; Lorenzelli, L. Piezoelectric Oxide Semiconductor Field Effect Transistor Touch Sensing Devices. *Appl. Phys. Lett.* **2009**, *95*, 034105.
10. Wang, X.; Wang, X.; Zhou, J.; Song, J.; Liu, J.; Xu, N.; Wang, Z. L. Piezoelectric Field Effect Transistor and Nanoforce Sensor Based on a Single ZnO Nanowire. *Nano Lett.* **2006**, *6*, 2768–2772.
11. Wang, Z. L. Nanopiezotronics. *Adv. Mater.* **2007**, *19*, 889–892.
12. Wang, Z. L. Progress in Piezotronics and Piezo-phototronics. *Adv. Mater.* **2012**, *24*, 4632–4646.
13. Wen, X.; Wu, W.; Ding, Y.; Wang, Z. L. Piezotronic Effect in Flexible Thin-Film Based Devices. *Adv. Mater.* **2013**, *25*, 3371–3379.
14. Wu, W.; Pan, C.; Zhang, Y.; Wen, X.; Wang, Z. L. Piezotronics and Piezo-phototronics: From Single Nanodevices to Array of Devices and Then to Integrated Functional System. *Nano Today* **2013**, *8*, 619–642.
15. Wang, X. Piezotronics: A New Field of Strain-Engineered Functional Semiconductor Devices. *Am. Ceram. Soc. Bull.* **2013**, *92*, 18–23.
16. Wang, Z. L.; Wu, W. Piezotronics and Piezo-phototronics: Fundamentals and Applications. *Natl. Sci. Rev.* **2014**, *1*, 62–90.
17. Zhou, J.; Gu, Y.; Fei, P.; Mai, W.; Gao, Y.; Yang, R.; Bao, G.; Wang, Z. L. Flexible Piezotronic Strain Sensor. *Nano Lett.* **2008**, *8*, 3035–3040.
18. Wu, W.; Wei, Y.; Wang, Z. L. Strain-Gated Piezotronic Logic Nanodevices. *Adv. Mater.* **2010**, *22*, 4711–4715.
19. Wu, W.; Wang, Z. L. Piezotronic Nanowire-Based Resistive Switches as Programmable Electromechanical Memories. *Nano Lett.* **2011**, *11*, 2779–2785.
20. Niu, S.; Hu, Y.; Wen, X.; Zhou, Y.; Zhang, F.; Lin, L.; Wang, S.; Wang, Z. L. Enhanced Performance of Flexible ZnO Nanowire Based Room-Temperature Oxygen Sensors by Piezotronic Effect. *Adv. Mater.* **2013**, *25*, 3701–3706.
21. Wu, W.; Wen, X.; Wang, Z. L. Taxel-Addressable Matrix of Vertical-Nanowire Piezotronic Transistors for Active and Adaptive Tactile Imaging. *Science* **2013**, *340*, 952–957.
22. Yu, R.; Pan, C.; Wang, Z. L. High Performance of ZnO Nanowire Protein Sensors Enhanced by the Piezotronic Effect. *Energy Environ. Sci.* **2013**, *6*, 494–499.
23. Fan, F. R.; Tian, Z. Q.; Wang, Z. L. Flexible Triboelectric Generator. *Nano Energy* **2012**, *1*, 328–334.
24. Wang, Z. L. Triboelectric Nanogenerators as New Energy Technology for Self-Powered Systems and as Active Mechanical and Chemical Sensors. *ACS Nano* **2013**, *7*, 9533–9557.
25. Zhang, C.; Zhou, T.; Tang, W.; Han, C.; Zhang, L.; Wang, Z. L. Rotating-Disk-Based Direct-Current Triboelectric Nanogenerator. *Adv. Energy Mater.* **2014**, *4*, 1301798.
26. Zhang, C.; Tang, W.; Han, C.; Fan, F.; Wang, Z. L. Theoretical Comparison, Equivalent Transformation, and Conjunction Operations of Electromagnetic Induction Generator and Triboelectric Nanogenerator for Harvesting Mechanical Energy. *Adv. Mater.* **2014**, *26*, 3580–3591.
27. Zhu, G.; Chen, J.; Zhang, T.; Jing, Q.; Wang, Z. L. Radial-Arrayed Rotary Electrification for High Performance Triboelectric Generator. *Nat. Commun.* **2014**, *5*, 3426.
28. Zhu, G.; Zhou, Y. S.; Bai, P.; Meng, X. S.; Jing, Q.; Chen, J.; Wang, Z. L. A Shape-Adaptive Thin-Film-Based Approach for 50% High-Efficiency Energy Generation through Micro-grating Sliding Electrification. *Adv. Mater.* **2014**, *26*, 3788–3796.
29. McCarty, L. S.; Whitesides, G. M. Electrostatic Charging Due to Separation of Ions at Interfaces: Contact Electrification of Ionic Electrets. *Angew. Chem., Int. Ed.* **2008**, *47*, 2188–2207.
30. Tans, S. J.; Verschueren, A. R.; Dekker, C. Room-Temperature Transistor Based on a Single Carbon Nanotube. *Nature* **1998**, *393*, 49–52.
31. Camara, C. G.; Escobar, J. V.; Hird, J. R.; Putterman, S. J. Correlation between Nanosecond X-ray Flashes and Stick-Slip Friction in Peeling Tape. *Nature* **2008**, *455*, 1089–1092.
32. Hird, J. R.; Camara, C. G.; Putterman, S. J. A Triboelectric X-ray Source. *Appl. Phys. Lett.* **2011**, *98*, 133501.